

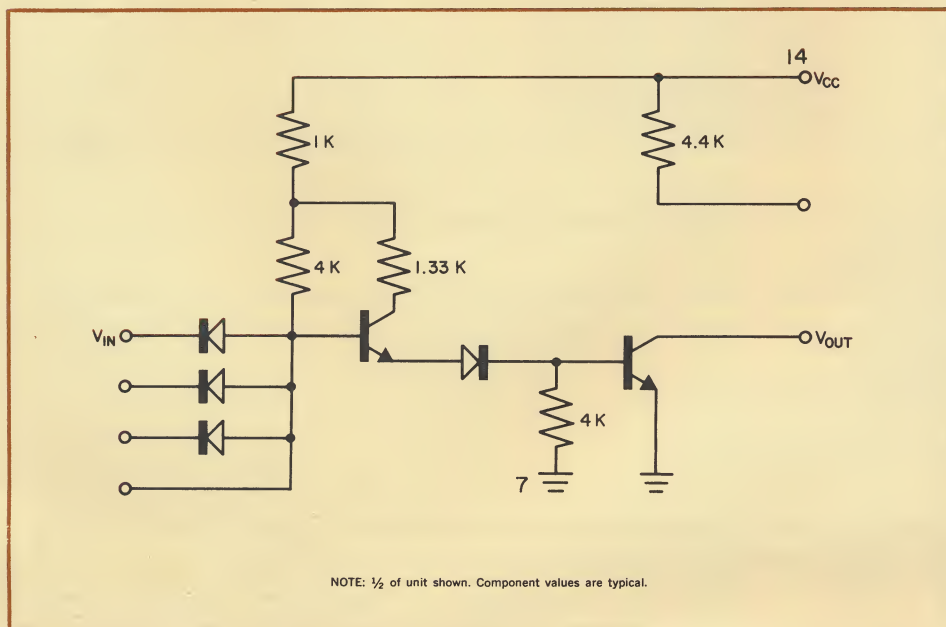
DUAL EXPANDABLE THREE-INPUT NAND GATE

LOW POWER MONOLITHIC DTL ELEMENT

The NE417A is a monolithic semiconductor integrated circuit designed for use in low power digital systems. This device offers an optional pull-up resistor allowing the flexibility of using wired "collector" logic applications. The element provides for input expansion utilizing expander elements from the NE100A logic family.

The same planar and epitaxial techniques used in fabricating the SE400J-Series elements are employed in making the NE400A-Series. These elements are tested under the appropriate portion of Signetics established SURE Program (Systematic Uniformity and Reliability Evaluation), as described in Bulletin No. 5001. Acceptance Test Sub-Groups called out in the tabular data refer to selection and test criteria as specified in Table II of SURE Program Bulletin No. 5001.

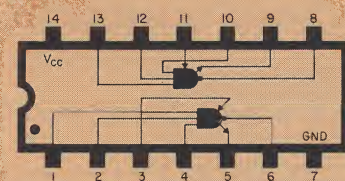
BASIC CIRCUIT SCHEMATIC



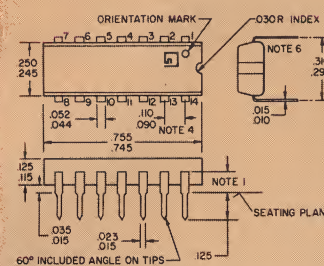
ABSOLUTE MAXIMUM RATINGS

INPUT VOLTAGE	6.0V
V _{CC}	6.0V
INPUT CURRENT	±10mA
OUTPUT CURRENT	+30, -10mA
OPERATING TEMPERATURE	0°C to +70°C
JUNCTION TEMPERATURE	150°C

Maximum ratings are limiting values above which serviceability may be impaired.



SIGNETICS A-PACKAGE



- NOTES: (1) Lead spacing shall be measured within this zone.
- (2) Molded Plastic Body.
- (3) Kovar Leads.
- (4) Lead spacing tolerances are non-cumulative.
- (5) Thermal resistance from junction to still air, $\Theta_{JA} = 0.16^{\circ}\text{C}/\text{mW}$.
- (6) Leads shown as positioned by Signetics dual in-line package carrier.
- (7) All dimensions of plastic package exclude molding-caused flash.



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NE417A

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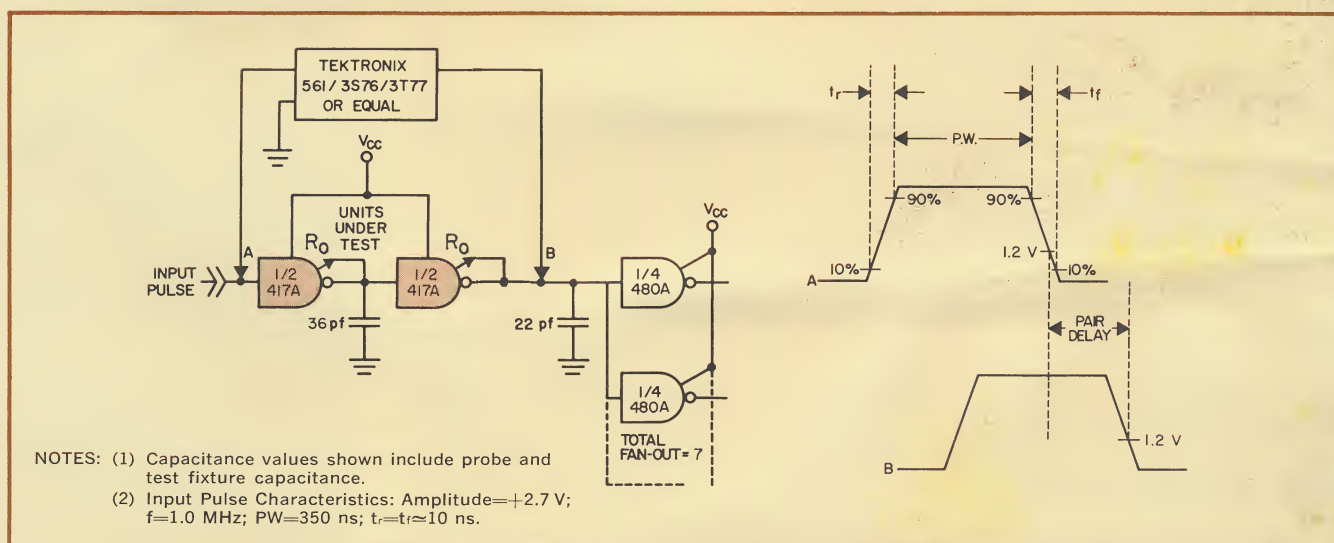
ELECTRICAL CHARACTERISTICS (NOTES: 1, 2, 3, 4, 5, 6, 12) $V_{CC} = 5.0V \pm 5\%$

ACCEPTANCE TEST SUB-GROUP	CHARACTERISTIC	LIMITS				TEST CONDITIONS				
		MIN.	TYP.	MAX.	UNITS	TEMP.	DRIVEN INPUT	OTHER INPUTS	OUTPUTS	NOTES
A-4	"1" OUTPUT CURRENT			25	μA	+70°C	0.8V			8
A-5	"0" OUTPUT VOLTAGE			0.35	V	0°C	2.0V	2.0V	7.0mA	8
A-3				0.35	V	+25°C	2.0V	2.0V	7.0mA	8
A-4				0.35	V	+70°C	2.0V	2.0V	7.0mA	8
C-1	"0" INPUT CURRENT			-1.5	mA	0°C	0.35V			
A-3				-1.5	mA	+25°C	0.35V			
C-1				-1.5	mA	+70°C	0.35V			
A-4	"1" INPUT CURRENT			25	μA	+70°C	5.0V	0V		
	PAIR DELAY (Figure 1)		65		ns	+25°C			DC F.O.=7	9
	INPUT CAPACITANCE		3.0		pf	+25°C	2.0V			7
	AVERAGE POWER CONSUMPTION PER GATE		9.0		mW	+25°C				11
A-2	INPUT VOLTAGE RATING	6.0			V	+25°C	50 μA	0V		
	DC FAN-OUT	7								9, 10
A-3	OUTPUT LOAD RESISTOR	3.5	4.4	5.3	K Ω	+25°C				

Notes:

- (1) All voltage and capacitance measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
- (2) All measurements are taken with Pin 7 tied to zero volts.
- (3) Positive current flow is defined as into the terminal referenced.
- (4) Positive NAND Logic definition: "UP" Level = "1", "DOWN" Level = "0".
- (5) Precautionary measures should be taken to ensure current limiting in accordance with maximum ratings should the isolation diodes become forward biased.
- (6) Measurements apply to each gate element independently.
- (7) Capacitance as measured on Boonton Electronic Corporation Model 75A-S8 Capacitance Bridge or equivalent, $f = 1 \text{ MHz}$, $V_{ac} = 25 \text{ mV}_{rms}$. All pins not specifically referenced are tied to guard for capacitance tests.
- (8) Optional pull-up resistor is not connected for this test.
- (9) DC fan-out is defined in terms of an NE480A gate input or an equivalent impedance.
- (10) This is not a test point, but is guaranteed as a result of calculations using guaranteed test points.
- (11) Measured at 50 percent duty cycle.
- (12) Manufacturer reserves right to make design changes and/or process improvements

FIGURE 1 — PAIR DELAY



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